What is claimed is:

1. Trench isolation structure of a semiconductor device comprising : a semiconductor substrate having an upper surface, and a trench extending into the substrate from said upper surface such that the substrate has upper corners where said upper surface and inner walls of the substrate that define the trench meet; and a trench isolation layer filling said trench, wherein the trench isolation layer and the semiconductor substrate contact each other at said upper corners along an interface, said interface having a rounded vertical sectional profile.

2. The trench isolation structure of claim 1, wherein said trench isolation layer comprises a first oxide layer buried in said trench, a buffer layer surrounding the first oxide layer, and a thermal oxide layer that contacts said buffer layer and said upper corners of the substrate, wherein said interface having a rounded vertical sectional profile exists between said thermal oxide layer and the semiconductor substrate.

3. The trench isolation structure of claim 2, wherein said rounded vertical sectional profile is in the shape of a bird's beak.

4. The trench isolation structure of claim 2, wherein said semiconductor substrate has a silicon-on-insulator (SOI) structure of respective layers that include a

silicon substrate, a buried oxide layer disposed on the silicon substrate, and a monocrystalline silicon layer disposed on the buried oxide layer.

5. The trench isolation layer of claim 4, wherein said trench terminates at an interface between two of the respective layers of said SOI structure.

6. The trench isolation layer of claim 2, wherein said buffer layer is one of a high temperature oxide layer, a middle temperature oxide layer and a plasma enhanced-oxide layer.

7. The trench isolation layer of claim 2, and further comprising a liner interposed between said buffer layer and said first oxide layer.

8. The trench isolation layer of claim 7, wherein said liner is one of a silicon nitride layer and a boron nitride layer.

9. The trench isolation layer of claim 7, and further comprising a second oxide layer interposed between said liner and said first oxide layer.

10. The trench isolation layer of claim 9, wherein said second oxide layer is one of a high temperature oxide layer, a middle temperature oxide layer and a plasma enhanced-oxide layer.

11. A method of manufacturing trench isolation structure of a semiconductor device, the method comprising the steps of:

(a) sequentially forming a pad oxide layer and a hard mask layer on a semiconductor substrate;

(b) patterning the hard mask layer and the pad oxide layer by photolithography to form a hard mask pattern and a pad oxide pattern;

(c) etching a portion of the semiconductor substrate using the hard mask pattern as a mask to thereby form a shallow trench;

(d) forming a thermal oxide layer along inner walls of the semiconductor substrate that define the shallow trench;

(e) etching away portions of the thermal oxide layer and the semiconductor substrate using the hard mask pattern as a mask to extend said shallow trench deeper into the semiconductor substrate and thereby form a deep trench;

(f) forming a buffer layer over the entire upper surface of the structure in which the deep trench has been formed;

(g) filling the deep trench, in which the buffer layer has been formed, with a first oxide layer;

(h) planarizing the resulting structure in which the deep trench has been filled with the first oxide layer; and

(i) removing the hard mask pattern.

12. The method of claim 11, and further comprising the step of forming a spacer along sidewalls of the hard mask pattern and the pad oxide pattern, and

wherein step (c) comprises etching a portion of the semiconductor substrate using the hard mask pattern and the spacer as a mask to thereby form the shallow trench, and step (e) comprises etching the thermal oxide layer and the semiconductor substrate using the hard mask pattern and the spacer as a mask to thereby form the deep trench.

13. The method of claim 11, and further comprising the step of forming a liner between the buffer layer and the first oxide layer.

14. The method of claim 12, and further comprising the step of forming a second oxide layer between the liner and the first oxide layer.

15. The method of claim 11, wherein the semiconductor substrate has a silicon-on-insulator (SOI) structure of respective layers that include a silicon substrate, a buried oxide layer, and a monocrystalline silicon layer disposed one atop the other, and wherein step (c) comprises terminating the etching of the semiconductor substrate at a location within the monocrystalline silicon layer in forming the shallow trench.

16. The method of claim 15, wherein step (e) comprises terminating the etching of the semiconductor substrate at an interface between two of the respective layers of the SOI structure in forming the deep trench.

17. A method of manufacturing a trench isolation layer, the method comprising the steps of:

(a) sequentially forming a pad oxide layer and a hard mask layer on an upper surface of a semiconductor substrate;

(b) patterning the hard mask layer and the pad oxide layer using photolithography to form a hard mask pattern and a pad oxide pattern;

(c) forming a thermal oxide layer on a portion of the upper surface of the semiconductor substrate where a trench isolation layer will be formed;

(d) etching away portions of the thermal oxide layer and the semiconductor substrate using the hard mask pattern as a mask to thereby form a deep trench;

(e) forming a buffer layer over the entire upper surface of the resulting structure in which the deep trench has been formed;

(f) filling the deep trench, in which the buffer layer has been formed, with a first oxide layer;

(g) planarizing the resulting structure in which the deep trench has been filled with the first oxide layer; and

(h) removing the hard mask pattern.

18. The method of claim 17, and further comprising the step of forming a spacer along sidewalls of the hard mask pattern and the pad oxide pattern, and wherein step (d) comprises etching the thermal oxide layer and the semiconductor substrate using the hard mask pattern and the spacer as a mask to thereby form the deep trench.

19. The method of claim 17, and further comprising the step of forming a liner between the buffer layer and the first oxide layer.

20. The method of claim 19, and further comprising the step of forming a second oxide layer between the liner and the first oxide layer.

21. The method of claim 17, wherein the semiconductor substrate has a silicon-on-insulator (SOI) structure of respective layers that include a silicon substrate, a buried oxide layer, and a monocrystalline silicon layer disposed one atop the other, and wherein step (d) comprises terminating the etching of the semiconductor substrate at an interface between two of the respective layers of the SOI structure in forming the deep trench.

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